



ΠΑΡΟΥΣΙΑΣΗ ΔΙΔΑΚΤΟΡΙΚΗΣ ΔΙΑΤΡΙΒΗΣ

- ΗΜΕΡΟΜΗΝΙΑ:** Πέμπτη, 22 Οκτωβρίου 2015
- ΩΡΑ:** 11:00
- ΑΙΘΟΥΣΑ:** Αίθουσα Σεμιναρίων
Κτήριο Τμήματος Μηχανικών Η/Υ & Πληροφορικής
- ΟΜΙΛΗΤΗΣ:** Γεώργιος Σφήκας

Θ έ μ α

«Fault Models, Test Algorithms and Embedded Test Techniques for DRAM Circuits»

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Περίληψη

Due to the revolutionary progress in the manufacturing process of Integrated Circuits (ICs) the last decades, electronic devices have become a part of everyday life. The direct results of this progress are the increased computing and storage capability of electronic devices, at an affordable or even low cost, and the mobility. However, although this progress rate has been constantly high for almost five decades, there are various threats to the further evolution of semiconductor technologies. One of the greatest threats is the rapidly increasing difficulty in testing ICs.

Dynamic Random Access Memories (DRAMs) are one of the most important parts in digital systems, both from a performance or a system failure perspective. Thus, their reliability is critical. Moreover, like in all IC technologies, the reliability issues grow more rapidly than the evolution of the manufacturing processes. Consequently, even if the manufacturing evolution is important, the development of new, more efficient and more reliable testing solutions turns out to be of equal importance.

The problems in testing and reliability of ICs mainly stem from the dimension shrinking of electronic components in order to integrate more devices in a small silicon area. In DRAMs, the shrinking of memory cells' dimensions and their in-between distances arise various undesired side effects. Among the most important side effects is the increased interaction between neighbouring cells. This interaction can cause complex faulty behaviors that are frequently hard to be detected because they appear only under the presence of specific conditions (e.g. the neighbouring cells are at a certain state).

The neighbouring cell interaction issue is addressed in this dissertation with two different approaches. In the first approach, we refine an existing fault model that deals with neighbouring cell interactions, the NPSF model, in order to provide test solutions with an acceptable cost in test application time. The test application time reduction achieved by our new test algorithm is 57.7% with respect to well known test algorithms that cover these faults. At the same time we provide test solutions for the cases where the NPSF faults are combined with the Bit-Line influence and Word-Line capacitive coupling related faults. In the second approach, we propose a new fault model, *the NLTF*, which targets specific well known interaction mechanisms. The test solution that derived from this new fault model further reduces the test application time up to 87% with respect to well known test algorithms that also cover these faults.

Another difficulty in DRAM memory testing is the fact that even the simplest defect can produce a quite complex faulty behavior. The main reason is that internally a DRAM operates like an analogue circuit. Electrical simulations of a DRAM with a resistive open defect manifested this complex faulty behavior. Moreover, we observed an important unknown phenomenon, the *charge accumulation*, that significantly influences the testing procedure. Based on our observations we developed an efficient test algorithm that provides enhanced coverage of resistive open faults.

One of the most attractive testing solutions is the Built-In Self-Test (BIST) circuits, which have gained great attention during the last two decades. Towards this direction, we have developed a BIST circuit that implements the NLTF test algorithm. The outcome of this task indicated the ability to efficiently embed complex test algorithms in a memory at a low silicon area and design cost. The functionality of the BIST circuit was verified through simulations.