ΔΙΑΛΕΞΗ

"Broadening the Research Avenues in Reconfigurable Computing and in Mixed-Criticality Systems"

Kyprianos D. Papadimitriou ,
Scientific staff
Technical University of Crete (TUC)
School of Electronic and Computer Engineering (ECE)

Περίληψη – Abstract

I will start with an introduction on reconfigurable computing technology and its most representative devices called Field Programmable Gate Arrays (FPGAs). FPGAs are integrated circuits consisting of a large array of uncommitted programmable logic and interconnect, plus large blocks such as memories and Digital Signal Processing (DSP) units that can be configured to implement digital circuits. Their capability to be programmed and reprogrammed in the field to form a digital circuit for executing the application at hand offers an unprecedented advantage over other technologies such as the Application Specific Integrated Circuits (ASICs) that cannot be reprogrammed, and the traditional software microprocessors in which flexibility comes at the expense of limited performance due to fixed instruction set and lack of parallelism. One of their promising feature is the ability to reuse the same hardware for different tasks at different phases of an application execution. Moreover, the tasks can be swapped "on the fly" while part of the hardware continues to operate. This feature is known as run-time or dynamic reconfiguration. Building upon the idea of dynamically reconfiguring a circuit in SRAM-based FPGAs, this talk presents architectural trade-offs of implementing applications in partially reconfigurable (PR) FPGA-based systems and proposes new avenues for its use. Initially, a novel way to schedule tasks in PR FPGAs is presented, which was evaluated within the context of a simulation framework. In addition, a real-world experimental framework was built, which was used as the basis to formulate a theoretical model for the early assessment of the reconfiguration overhead. I will then describe a novel way to exploit the PR technology in a specific application domain. All aspects of the present research have been verified with experiments from different setups using partially reconfigurable FPGA platforms. I will continue with my latest research, which includes the development of a runtime manager for servicing systems combining software and reconfigurable hardware, and the use of on-chip networks in mixed-criticality systems.

Kyprianos Papadimitriou is with the School of Electronic and Computer Engineering, Technical University of Crete. His experience ranges from working in the industry and conducting research in academic institutions, to lecturing and lab-teaching in the fields of digital design and circuits, computer hardware, and computer architecture. His research interests are in the areas of Reconfigurable Computing, Microcontrollers, Hardware Design, Run-time Systems, Real-Time Systems, Application Acceleration, Reliability, and On-Chip Interconnect. He defended his PhD in January 2012, and took his MSc degree in June 2003. After his undergraduate studies, from March 1998 to June 1999 he worked for ATMEL Corp. on hardware design and implementation of wireless protocols, mainly on Bluetooth technology. After his M.Sc, from October 2003 to May 2005, he was awarded with a national grant for exploiting the outcome of his master thesis through a spin-off company. From September 2011 to November 2014 he worked as a Research Associate at FORTH-ICS; he was invited for this position in order to support the research and coordination of a project relevant to his PhD area. Kyprianos Papadimitriou holds a US patent and has published over 40 papers in

international journals and conferences. He is co-author of a paper nominated for Best award in the 21st IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC) in 2013, and co-inventor of one of the first technologies developed at TU Crete that got patent filing in US (2005). In 2004 he was nominated for an award in Michael Dertouzos Competion, XIV World Congress on Information Technology (WCIT), and in 1998 he received the 3rd Award of Excellence in Telecommunications from Ericcsson Hellas for his diploma thesis. He is serving the technical program committees of 3 Conferences/Symposiums in his field, the International Conference on Field-Programmable Logic and Applications (FPL), the International Conference on ReConFigurable Computing and FPGAs (ReConFig), and the International Symposium on Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC), and he is in the review board of journals of IEEE, ACM, Elsevier and Springer. He was session chair in Workshops of two International Conferences, IEEE Conference on Communications and Network Security (CNS) and IEEE High Performance Computing and Communications (HPCC). He has participated in 4 EU and 4 National funded research projects; in one of them he was the Principal Investigator and in another one Technical Manager. Besides these projects, he has supported with his work and publications 4 more projects, in which he didn't have a formal relation via a contract. Currently he is laboratory and teaching staff at the School of Electronic and Computer Engineering, Technical University of Crete, and since January 2014 he is affiliated with the Technological Educational Institute of Crete. He is elected member in the Representative Board of Electronic and Computer Engineers, Central Delegation of the Technical Chamber of Greece.

Παρασκευή 17/6/2016 – 12:00

Αίθουσα Σεμιναρίων,

Κτίριο Μηχανικών Η/Υ & Πληροφορικής

Πανεπιστήμιο Ιωαννίνων